AMENDMENTS TO THE SPECIFICATION

Please amend the specification, as follows:

Replace paragraph [0025] with the following amended paragraph [0025]:

The Modulus recoder 220 can output multiple signals (e.g., a multiple modulus selection signal SEL_MM[1:0], a multiple modulus negation indicating signal NEG_MM, . . .). In an exemplary embodiment of the present invention, the Modulus recoder 220 outputs SEL_MM[1:0] to the multiplexer 230, which uses the value of SEL_MM[1:0] to select one of four possible values of MM_I (e.g., 2M, M, 0, M). The multiplexer (MUX) 230 inputs the modulus M and, in an exemplary embodiment, two LSBs of the multiple modulus selection signal SEL_MM[1:0], outputting the value of MM_I. MM_I is sent to the accumulator 250. The multiple modulus negation indicating signal NEG_MM can be combined in a half adder 47 with the partial product negation indicating signal NEG_PP to obtain the ~~compensatory~~ compensating word signal CW. CW is sent to the accumulator 250.

Replace paragraph [0032] with the following amended paragraph [0032]:

An exemplary accumulator 500 in accordance with the present invention is illustrated in Figure 5. The accumulator is composed of n+2 series of 5-2 compressors in a compress network 505, broken into full compressors (e.g., [[520]] 510) and reduced compressors (e.g., [[510]] 570), where n is the bit length of modulus value M. The accumulator 500 stores sum (S) and carry (C) values in a sum register 530 (S_REG) and a carry register 540 (C_REG),

respectively. The outputs of the S_REG 530 and the C_REG 540 are input to a carry propagation adder 550, which converts a redundant number to a normal number, storing the value in a final register 560 (F_REG).

Replace paragraph [0033] with the following amended paragraph [0033]:

Input to the accumulator 500, in an exemplary embodiment of the present invention, are compensating word CW[1:0], the multiple modulus value MM_I, and the partial product value PP_I. The first two full compressors, [[570]] 510 and 520, input CW[1:0] along with MM_I[1:0] and PP_I[1:0]. The remaining reduced compressors [[510]] 570, 580, 590, etc., use the remaining bits of the multiple modulus value MM_I[n+1:2], and the partial product value PP_I[n+1:2]. The last compressor 580 (n+2 compressor) prevents overflow and the first compressor [[570]] 510 (n=0) is a full compressor missing a third full adder. Other exemplary embodiments can have a various number of bits for the various variable values (e.g., CW, MM_I, PP_I, . . .) and discussion herein should not be interpreted to limit the bit sizes of the variables.

Replace paragraph [0037] with the following amended paragraph [0037]:

In an exemplary embodiment of the present invention, the full compressor 600 is composed of three full adders. The first full adder 610 inputs the values C_I, S_I, and CW and outputs a first full adder carry (FCO1) and a first full adder sum (FSO1). FCO1 serves as a first output carry CO1, which can be a secondary first input CI1[k+1] for the next-higher-bit compressor (k+1). The second full adder 620 inputs FSO1, the partial product bit value PP_I[k]

and the multiple modulus bit value $MM_I[k]$ associated with the bit designation (k) of the compressor. The second full adder 620 outputs a second full adder carry (FCO2) and a second full adder sum (FSO2). FCO2 serves as a first output carry CO2, which can be a secondary second input CI2[k+1] for the next-higher-bit compressor (k+1). The third full adder 630 inputs FSO2, and CI1[k-1] and CI2[k-1] from a lower-bit compressor (k-1). The third full adder 630 outputs a third full adder carry (FCO3) and a third full adder sum (FSO3). FCO3 serves as the next carry word bit value C_{I+1}, which is used to obtain the input C_I to a lower-bit compressor (k-1). FSO3 serves as the next sum word S_{I+1}, which is used to obtain the input S_I to a two-bits-lower compressor (k-2). The first full compressor [[570]] 510 corresponding to bit 0 does not output next carry or sum words, thus the third full adder is not needed. Likewise, the second full compressor 520 corresponding to bit 1 does not output a next sum word bit value.

Replace paragraph [0038] with the following amended paragraph [0038]:

The compensating word CW[1:0] has two bits and thus requires two compressors, one for each bit. Thus, the first two compressors, [[570]] 510 and 520, are full compressors inputting a plurality of values. In exemplary embodiments, the full compressors [[570]] 510 and 520 input five values. The higher bit compressors ~~[2:n+2]~~ [n+2:2] input a plurality of values that are less than that input to compressors [[570]] 510 and 520, and are referred to as reduced compressors [[510]] 570, 580, 590, etc. Reduced compressors replace the first full adder with a half adder. Thus, the half adder 710 in the reduced compressor inputs the values C_I and S_I, and outputs a first half adder carry (HCO1) and a first half adder sum (HSO1). HCO1 serves as a first output carry CO1, which can be a secondary first input CI1[k+1] for the next-higher-bit compressor

(k+1). The second full adder 720 inputs HSO1, the partial product bit value $PP_I[k]$ and the multiple modulus bit value $MM_I[k]$ associated with the bit designation (k) of the compressor. The second full adder 720 outputs a second full adder carry (FCO2) and a second full adder sum (FSO2). FCO2 serves as a second output carry CO2, which can be a secondary second input CI2[k+1] for the next-higher-bit compressor (k+1). The third full adder 730 inputs FSO2, and CI1[k-1] and CI2[k-1] from a lower-bit compressor (k-1). The third full adder 730 outputs a third full adder carry (FCO3) and a third full adder sum (FSO3). FCO3 serves as the next carry word bit C_{I+1}, which serves as input C_I to a lower bit compressor (k-1) after passing to the carry register 540. FSO3 serves as the next sum word bit S_{I+1}, which serves as input S_I to a two-bits-lower compressor (k-2) after passing to the sum register 530.

Replace paragraph [0039] with the following amended paragraph [0039]:

The accumulator 500 of Figure 5, in accordance with an exemplary embodiment of the present invention, links in series full compressors and reduced compressors, the number of which depends on the input bit size of the multiple modulus value (MM_I) and the partial product value (PP_I). The two LSB compressors are full compressors that use the compensating word (CW) as an input. The first bit compressor [[570]] 510 outputs CO1[0] and CO2[0], which become secondary inputs to the next-higher-bit (second bit) compressor 520, CI1[1] and CI2[1] respectively. This continues until the highest-bit compressor (n+2), which does not output carry outputs (CO1[n+2] and CO2[n+2]). The highest-bit compressor prevents overflow and its secondary inputs are obtained from its own next carry word bit and next sum word bit values.

Replace paragraph [0043] with the following amended paragraph [0043]:

The multiplexers (MXG_{n+1} to MXG_0) can control the electrical connections between full adders in the compressors. As shown in Figure 8, the first two bit compressors [[870]] 810 and 820 in a compress network 805 are analogous to the description and operation of the compressors 510 and 520 ~~and 570~~, respectively, except that the next carry word bit value ($C_{I+1}[k]$) is not only passed to the carry register 840 to obtain a current carry word bit value $C_I[k-1]$, used by the lower bit compressor [[870]] 810, $C_{I+1}[k]$ is passed to the next-higher-bit compressor [k+1] as input to a multiplexer associated with the higher-bit compressor MXG_{k-2}.